WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a P-poly gate and an N-poly gate on a P type element region and an N element region, respectively, of a semiconductor substrate electrically isolated by an element isolating layer;

shielding the P type element region and lightly ion-doping the N type impurities selectively to a predetermined N-LDD region around the N-poly gate;

forming an oxide layer for regulating the ion-implantation on the front face of the semiconductor substrate so as to cover the P-poly gate and the N-poly gate;

shielding the N type element region and lightly ion-doping the P type impurities selectively to a predetermined P-LDD region around the P-poly gate using the oxide layer for regulating the ion-implantation as a buffer mask;

removing the oxide layer for regulating the ion-implantation, forming spacers to the respective P-poly gate and the N-poly gate, and heavily ion-doping the P type and N type impurities selectively to a predetermined P-source/drain region and a predetermined N-source/drain region around the P-poly gate and the N-poly gate, respectively, using the respective spacers as buffer masks; and

annealing the semiconductor substrate so as to diffuse the P type and N type impurities doped to the predetermined P-LDD and N-LDD regions and the predetermined P-source/drain and N-source/drain regions.

2. The method of claim 1, wherein the oxide layer for regulating the ion-implantation is formed by a PECVD process at the temperature of 200~400℃.

3. The method of claim 1, wherein the oxide layer for regulating the ion-implantation is a Tetra Ethyl Ortho Silicate (TEOS) film.

4. The method of claim 1, wherein the oxide layer for regulating the ion-implantation has the thickness of 100~500 Å.

5. A method of manufacturing a semiconductor device, comprising:

forming a P-poly gate and an N-poly gate on a P type element region and an N element region, respectively, of a semiconductor substrate electrically isolated by an element isolating layer;

forming an oxide layer for a spacer on the front face of the semiconductor substrate so as to cover the P-poly gate

and the N-poly gate;

shielding the N type element region, patterning the oxide layer for the spacer formed on the P type element region to form a first scale P-spacer on a sidewall of the P-poly gate, and lightly ion-doping the P type impurities selectively to a predetermined P-LDD region around the P-poly gate using the P-spacer as a buffer mask;

shielding the P type element region, patterning the oxide layer for the spacer formed on the N type element region to form a second scale N-spacer on a sidewall of the N-poly gate, and lightly ion-doping the N type impurities selectively to a predetermined N-LDD region around the N-poly gate using the N-spacer as a buffer mask;

heavily ion-doping the P type and N type impurities selectively to a predetermined P-source/drain region and a predetermined N-source/drain region around the P-poly gate and the N-poly gate, respectively; and

annealing the semiconductor substrate so as to diffuse the P type and N type impurities doped to the predetermined P-LDD and N-LDD regions and the predetermined P-source/drain and N-source/drain regions.

6. The method of claim 5, wherein the oxide layer for spacer is formed at the temperature of 700~900℃.

7. The method of claim 5, wherein the oxide layer for spacer has the thickness of 100~500Å.